

AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listing of claims in the application.

Claims 1-6, 8 and 10-20 remain in this application.

Claims 1, 4-6 and 8 are being amended.

WHAT IS CLAIMED IS:

1. (Currently Amended) A modulator for receiving sample values and generating digital signals using selectable programs for implementing respective delta sigma algorithms, a topology of the delta sigma modulator including a set of arithmetic and logic blocks configurable in response to at least one program to implement a corresponding one of the delta sigma algorithms.
2. (Previously Presented) The modulator of claim 1 in which at the least one program generates a delta sigma algorithm of selectable order N , where N is an integer greater than or equal to one.
3. (Original) The modulator of claim 1 in which said sample values are stored into a first in first out memory element.
4. (Currently Amended) An integrated circuit containing a delta sigma modulator programmable to implement different delta sigma algorithms, a topology of the delta sigma modulator including a set of arithmetic and logic blocks configurable in response to at least one program to implement a corresponding one of the delta sigma algorithms.
5. (Currently Amended) An integrated circuit containing a delta sigma modulator programmable to implement different delta sigma sampling rates, the delta sigma modulator having a topology including a set of arithmetic and logic blocks configurable in response to a

selected program to select a delta sigma data rate.

6. (Currently Amended) A method of designing an integrated circuit, comprising the step of providing a programmable delta sigma modulator, the programmable delta sigma modulator having a topology including a set of arithmetic and logic blocks configurable in response to at least one program to implement a corresponding delta sigma algorithm.

7. (Cancelled)

8. (Currently Amended) A method of fabricating an integrated circuit, comprising the step of providing a programmable delta sigma modulator, the programmable delta sigma modulator having a topology including a set of arithmetic and logic blocks configurable in response to at least one program to implement a corresponding one delta sigma algorithm.

9. (Cancelled)

10. (Previously Presented) The modulator of claim 2, in which an algorithm of order N is implemented by selecting a coefficient set from among plural coefficient sets.

11. (Previously Presented) The integrated circuit of claim 4 in which different algorithms are implemented using by changing a particular architecture of corresponding circuitry used to perform operations in response to at least one control signal.

12. (Original) The integrated circuit of claim 11 in which a particular architecture is a one using multipliers.

13. (Original) The integrated circuit of claim 11 in which a particular architecture is a one using no multipliers but only shifts and adds.

14. (Original) The integrated circuit of claim 11 in which a particular architecture is a one using a pipelined architecture.
15. (Original) The integrated circuit of claim 11 in which a particular architecture is a one using a hybrid memory system.
16. (Original) The integrated circuit of claim 11 in which a particular architecture is a one using a register file arrangement.
17. (Previously Presented) The integrated circuit of claim 11 in which said at least one control signal is provided by a sequencer.
18. (Original) The integrated circuit of claim 4 in which said delta-sigma modulator has an output with controllable delays.
19. (Original) The integrated circuit of claim 4 having two delta sigma modulators, each having an independently controllable output delay.
20. (Original) The integrated circuit of claim 19 in which the independently controllable delay is a serial shift register with a selectable number of active stages.
21. (Cancelled).